High Speed, ±100V 2.5A, Two or Three Level Ultrasound Pulser

Features

- HVCMOS® technology for high performance
- High density integration AC coupled pulser
- 0 to ±100V output voltage
- ±2.5A source and sink minimum pulse current
- Up to 35MHz operating frequency
- 2.0ns matched delay times
- 2.5, 3.3 or 5.0V CMOS logic interface
- Low power consumption and very simple to use

Application

- Medical ultrasound imaging
- Piezoelectric transducer drivers
- NDT ultrasound transmission
- Pulse waveform generator

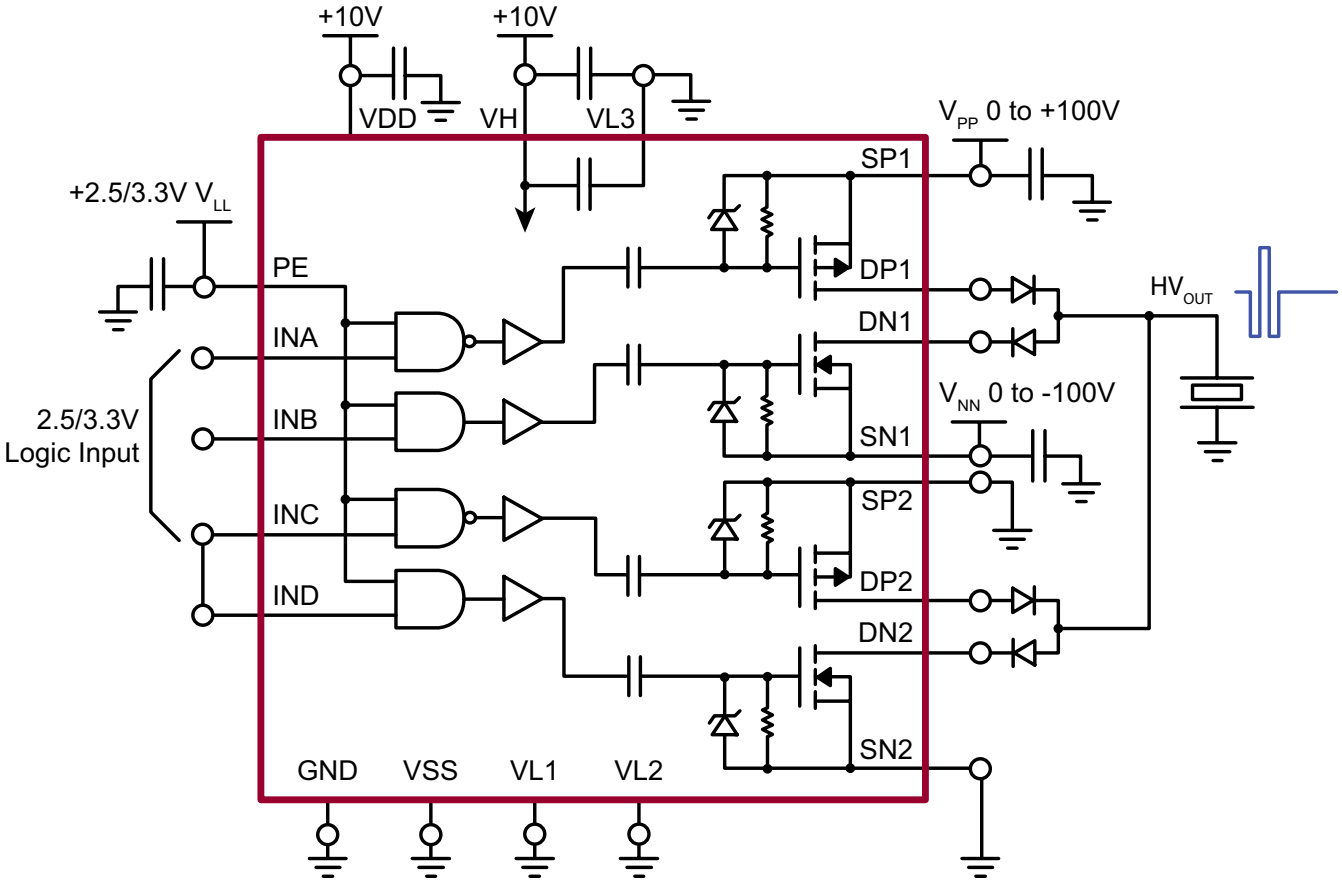
General Description

The Supertex HV7360 is a high voltage, high-speed, pulse generator with built-in, fast return to zero damping FETs. This high voltage and high-speed integrated circuit is designed for portable medical ultrasound image devices, but can also can be used for NDT and test equipment applications.

The HV7360 consists of a controller logic interface circuit, level translators, AC coupled MOSFET gate drivers and high voltage and high current P-channel and N-channel MOSFETs as the output stage.

The peak output currents of each channel are guaranteed to be over ±2.5A with up to ±100V of pulse swing. The AC coupling topology for the gate drivers not only saves two floating voltage supplies, it also makes the PCB layout easier.

Typical RTZ Application Circuit



Ordering Information

Part Number	Package Option	Packing
HV7360LA-G	22-Lead LFGA	364/Tray

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

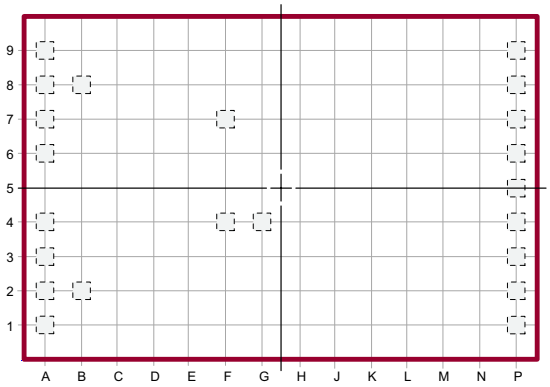
Parameter	Value
V_{DD} – V_{SS} Logic supply voltage	-0.5 to +12.5V
V_H Output high supply voltage	V_L -0.5 to V_{DD} +0.5V
V_L Output low supply voltage	V_{SS} -0.5V to V_H +0.5V
V_{SS} Low side supply voltage	-6.0 to +0.5V
(V_{SPx} - V_{SNx}) Differential high voltage	+220V
V_{SPx} Positive high voltage	-0.5 to +110V
V_{SNx} Negative high voltage	+0.5 to -110V
All logic input voltages	V_{SS} -0.5V to GND +5.5V
Coupling capacitor breakdown voltage	±110V
Maximum junction temperature	125°C
Operating temperature	-20 to +85°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Typical Thermal Resistance

Package	θ_{ja}
22-Lead LFGA	106°C/W

Pad Configuration



22-Lead LFGA (LA)
(top view)

Package Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
___ = "Green" Packaging

Package may or may not include the following marks: Si or

22-Lead LFGA (LA)

Power-Up Sequence

Step	Description
1	V_{LL}
2	V_{DD}, V_H, V_{SS}, V_L with signal logic low
3	V_{PP} and V_{NN}
4	PE active

Power-Down Sequence

Step	Description
1	PE inactive
2	V_{PP} and V_{NN} off
3	V_{DD}, V_H, V_{SS}, V_L off
4	V_{LL} off

Note:
Powering up/down in any arbitrary sequence will not cause any damage to the device. The powering up/down sequence is only recommended in order to minimize possible inrush current.

Logic Control Table

PE	Input Pulse				Output MOSFETs			
	INA	INB	INC	IND	SP1 to DP1	DN1 to SN1	SP2 to DP2	DN2 to SN2
1	**1**	X	X	X	**ON**	X	X	X
	X	**1**	X	X	X	**ON**	X	X
	X	X	**1**	X	X	X	**ON**	X
	X	X	X	**1**	X	X	X	**ON**
	0	X	X	X	**OFF**	X	X	X
	X	**0**	X	X	X	**OFF**	X	X
	X	X	**0**	X	X	X	**OFF**	X
	X	X	X	**0**	X	X	X	**OFF**
0	X	X	X	X	OFF	OFF	OFF	OFF

Operating Supply Voltages and Current

(Operating conditions, unless otherwise specified, GND = 0V, $V_H = V_{DD}$ = +10V, $V_L = V_{SS}$ = 0V, V_{PE} = 3.3V, V_{PP} = +100V, V_{NN} = -100V, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Unit	Conditions
$V_{DD} - V_{SS}$	Supply voltage	4.75	-	11.50	V	$4.0 \le V_{DD} \le 11.5V$
V_{SS}	Low side supply voltage	-5.5	-	0	V	---
V_H	Output high supply voltage	V_{SS} +4.0	-	V_{DD}	V	$V_H - V_L \ge 4.0V$
V_L	Output low supply voltage	V_{SS}	-	V_{DD} -4.0	V	
I_{DDQ}	V_{DD} quiescent current	-	50	-	µA	No input transitions, PE = 0
I_{HQ}	V_H quiescent current	-	2.0	-	µA	
I_{DDQ}	V_{DD} quiescent current	-	1.0	-	mA	No input transitions, PE = 1
I_{HQ}	V_H quiescent current	-	2.0	-	µA	
I_{DD}	V_{DD} average current	-	4.0	-	mA	One channel ON at 5.0Mhz, No load
I_H	V_H average current	-	10	-	mA	
V_{IH}	Input logic voltage high	V_{PE} -0.3	-	V_{PE}	V	For logic inputs INA, INB, INC, and IND
V_{IL}	Input logic voltage low	0	-	0.3	V	
I_{IH}	Input logic current high	-	-	1.0	µA	
I_{IL}	Input logic current low	-	-	1.0	µA	
V_{PEH}	PE input logic voltage high	1.70	3.30	5.25	V	For logic input PE
V_{PEL}	PE input logic voltage low	0	-	0.3	V	
R_{INPE}	PE input impedance to GND	100	-	-	kΩ	

AC Electrical Characteristics

(Operating conditions, unless otherwise specified, GND = 0V, $V_H = V_{DD}$ = +10V, $V_L = V_{SS}$ = 0V, V_{PE} = 3.3V, V_{PP} = +100V, V_{NN} = -100V, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Unit	Conditions
t_{irf}	Input or PE rise & fall time	-	-	10	ns	Logic input edge speed requirement
t_{d1-4}	Input to output delay	-	7.5	-	ns	R_{LOAD} = 1.0Ω
$t_{r/f1-2}$	Output rise/fall time	-	9.5	-	ns	C_{LOAD} = 330pF, R_{LOAD} = 2.5kΩ
Δt_{rf}	Rise and fall time matching	-	2.0	-	ns	Channel to channel
Δt_{dC2C}	Propagation matching	-	1.0	-		
Δt_{dD2D}	Propagation delay matching	-	±2.0	-	ns	Device to device delay match
t_{PE-ON}	PE ON-time	-	-	5.0	µs	V_{PE} = 1.7 ~ 5.25V V_{DD} = 7.5 ~ 11.5V -20 ~ 85°C
t_{PE-OFF}	PE OFF-time	-	-	4.0		
C_{OG}	Output to MOSFET gate cap	-	10	-	nF	100V X7S
C_{VH}	V_H to V_{L3} decoupling cap	-	0.22	-	µF	16V X7R

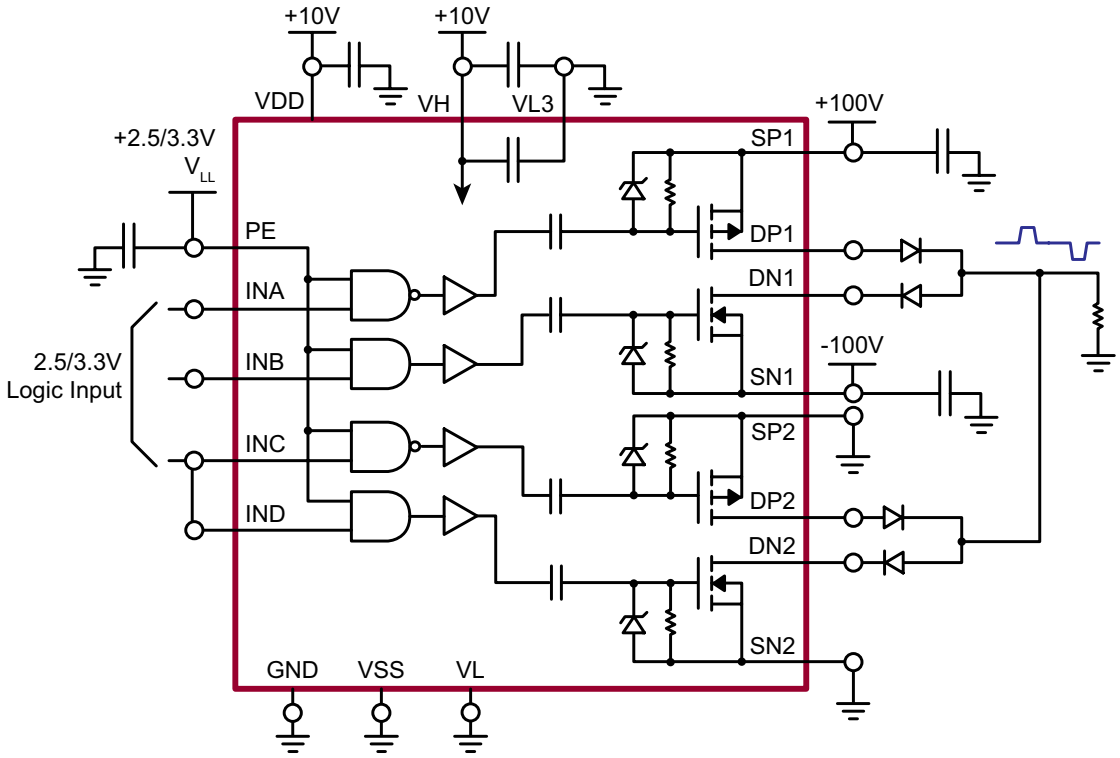
Pulser & Damping P-Channel MOSFET

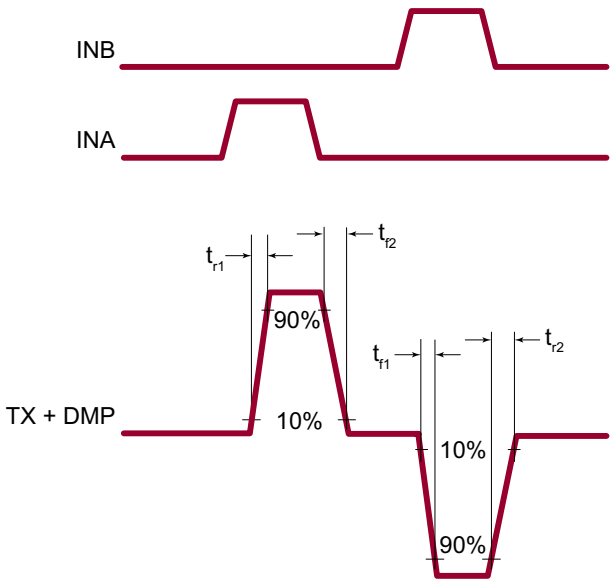
Sym	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-200	-	-	V	V_{GS} = 0V, I_D = -2.0mA
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.4	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	4.5	mV/^{O}C	V_{GS} = V_{DS}, I_D = -1.0mA
R_{GS}	Gate-to-source shunt resistor	10	-	50	kΩ	I_{GS} = 100µA, if applied
V_{ZGS}	Gate-to-source Zener voltage	13.2	-	25	V	I_{GS} = -2.0mA, if applied
I_{DSS}	Zero gate voltage drain current	-	-	-10	µA	V_{DS} = max rating, V_{GS} = 0V
		-	-	-1.0	mA	V_{DS} = 0.8max rating, V_{GS} = 0V, T_A = 125^{O}C
$I_{D(ON)}$	ON-state drain current	-1.2	-	-	A	V_{GS} = -5.0V, V_{DS} = -25V
		-2.3	-2.5	-		V_{GS} = -10V, V_{DS} = -50V
$R_{DS(ON)}$	Static drain-to-source ON-state resistance	-	-	8.5	Ω	V_{GS} = -5.0V, I_D = -150mA
		-	-	7.0		V_{GS} = -10V, I_D = -1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.0	%/^{O}C	V_{GS} = -10V, I_D = -1.0mA
G_{FS}	Forward transconductance	400	-	-	mmho	V_{DS} = -25V, I_D = -500mA
C_{ISS}	Input capacitance	-	75	-	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	21	-		
C_{RSS}	Reverse transfer capacitance	-	6.5	-		
V_{SBD}	Diode forward voltage drop and reverse recovery time of body-diode	-	-	1.8	V	V_{GS} = 0V, I_{SD} = 500mA
t_{rrBD}		-	300	-	ns	---

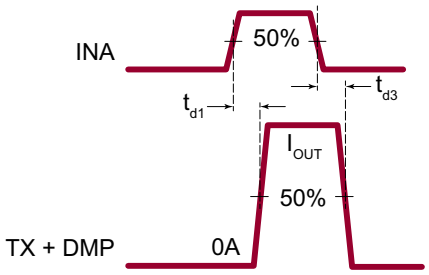
Pulser & Damping N-Channel MOSFET

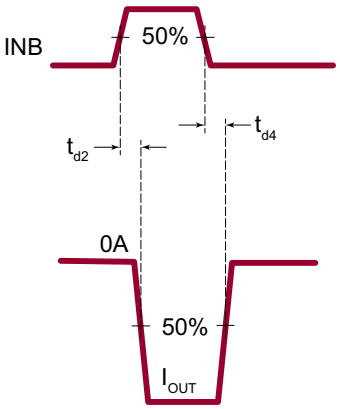
Sym	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	200	-	-	V	V_{GS} = 0V, I_D = 2.0mA
$V_{GS(th)}$	Gate threshold voltage	1.0	-	2.4	V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	-4.5	mV/^{O}C	V_{GS} = V_{DS}, I_D = 1.0mA
R_{GS}	Gate-to-source shunt resistor	10	-	50	kΩ	I_{GS} = 100µA
V_{ZGS}	Gate-to-source Zener voltage	13.2	-	25	V	I_{GS} = 2.0mA
I_{DSS}	Zero gate voltage drain current	-	-	10	µA	V_{DS} = max rating, V_{GS} = 0V
		-	-	1.0	mA	V_{DS} = 0.8max rating, V_{GS} = 0V, T_A = 125^{O}C
$I_{D(ON)}$	ON-state drain current	1.3	-	-	A	V_{GS} = 5.0V, V_{DS} = 25V
		2.3	2.5	-		V_{GS} = 10V, V_{DS} = 50V
$R_{DS(ON)}$	Static drain-to-source ON-state resistance	-	-	6.5	Ω	V_{GS} = 5.0V, I_D = 150mA
		-	-	6.0		V_{GS} = 10V, I_D = 1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.0	%/^{O}C	V_{GS} = 10V, I_D = 1.0A
G_{FS}	Forward transconductance	400	-	-	mmho	V_{DS} = 25V, I_D = 500mA
C_{ISS}	Input capacitance	-	56	-	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	13	-		
C_{RSS}	Reverse transfer capacitance	-	2.0	-		
V_{SBD}	Diode forward voltage drop and reverse recovery time of body-diode	-	-	1.8	V	V_{GS} = 0V, I_{SD} = 500mA
t_{rrBD}		-	300	-	ns	---

Switch Timing and Delay Test

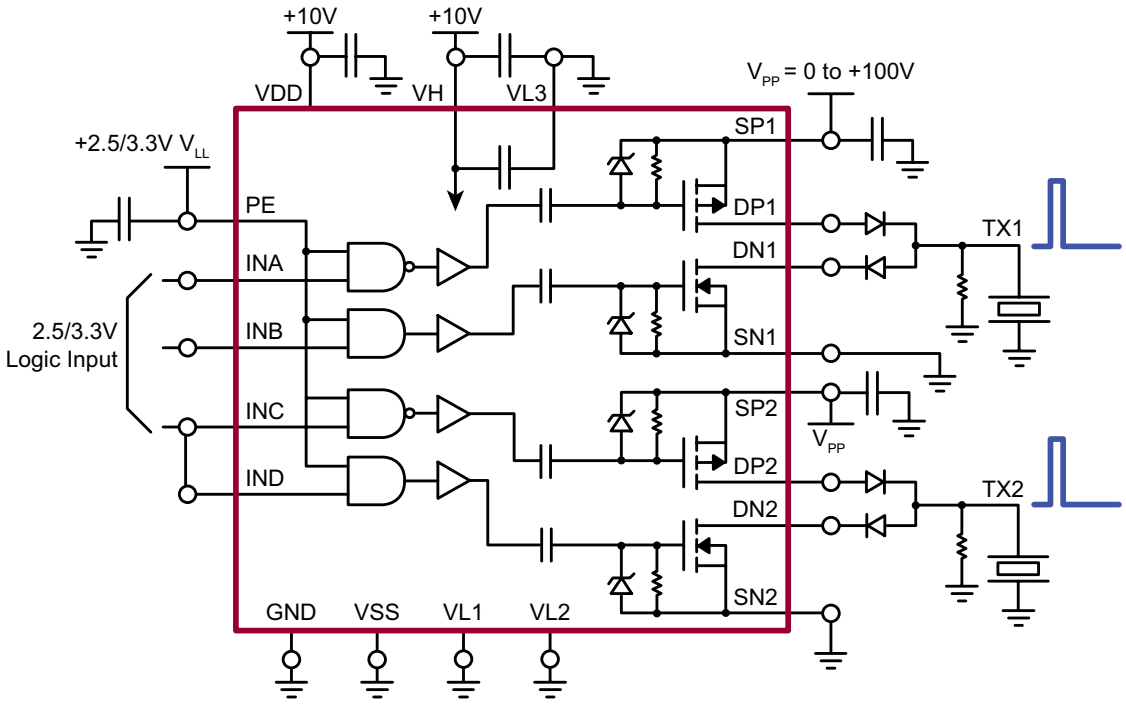








Typical Unipolar 2-Channel Application Circuit



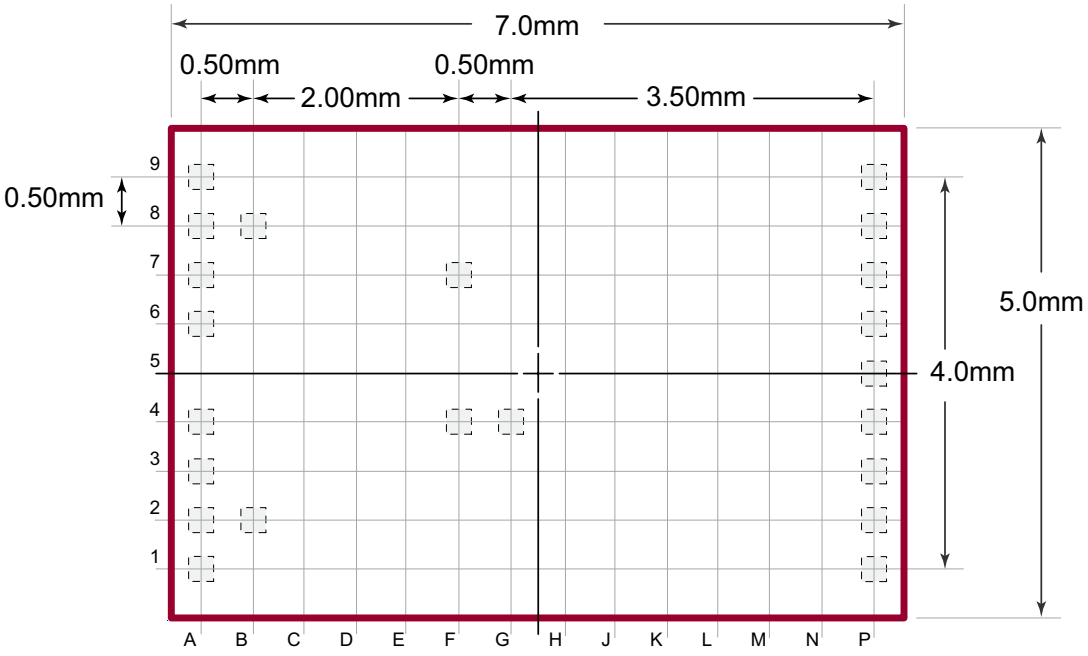
Pad Description

Pad Location	Name	Function
A1	GND	Driver and level translator circuit ground return (0V)
A2	IND	Damping N-FET control signal logic Input, controlling N-FET2
A3	INC	Damping P-FET control signal logic Input, controlling P-FET2
A4	VSS	Negative voltage power supply (0V)
A6	VDD	Positive voltage supply (+10V), should connect to an external decoupling cap to VSS (0V)
A7	INB	Pulsing N-FET control signal logic Input, controlling N-FET1
A8	INA	Pulsing P-FET control signal logic Input, controlling P-FET1
A9	PE	Drive power enable Hi = ON, Low = OFF , logic “1” voltage reference input (+1.8 to +3.3V)
B2	VL2	Gate-Drive negative voltage power supply (0V)
B8	VL1	Gate-Drive negative voltage power supply (0V)
F4	VH	Gate driver positive voltage power supply (+10V)
F7	VL3	VH to VL decoupling cap, should connect to VL1 & VL2 (0V) ground plane as short as possible
G4	NC	Do not connect
P1	SP2	Source of P-FET2, positive high voltage power supply (0 to +100V) or GND
P2	DP2	Drain of P-FET2, transmit pulser output
P3	DN2	Drain of N-FET2, transmit pulser output

Pad Description *(cont.)*

Pad Location	Name	Function
P4	SN2	Source of N-FET2, negative high voltage power supply (0 to -100V) or GND
P5	NC	Do not connect
P6	SP1	Source of P-FET1, positive high voltage power supply (0 to +100V)
P7	DP1	Drain of P-FET1, transmit pulser output
P8	DN1	Drain of N-FET1, transmit pulser output
P9	SN1	Source of N-FET1, negative high voltage power supply (0 to -100V)

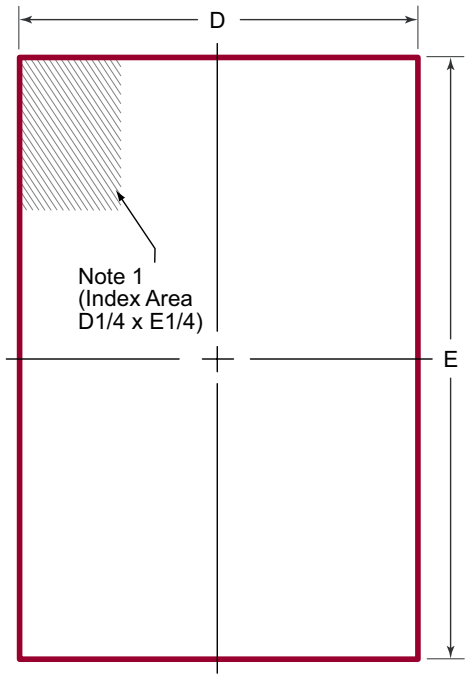
Pad Configuration



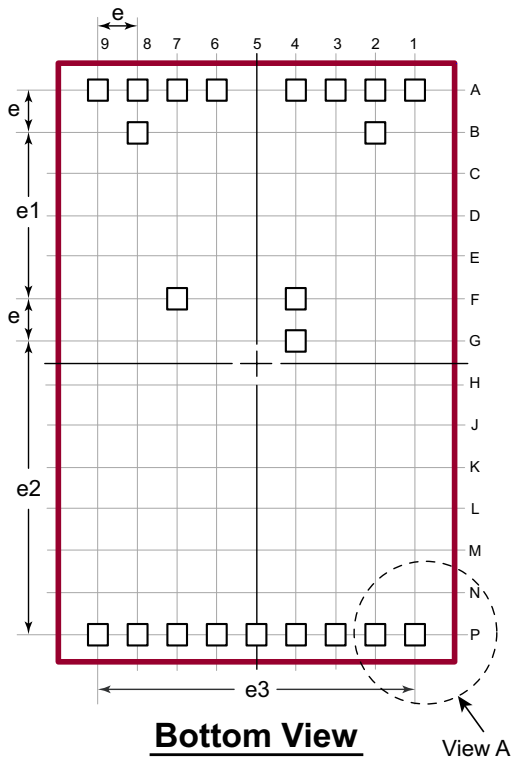
(Top View)

22-Lead LFGA Package Outline (LA)

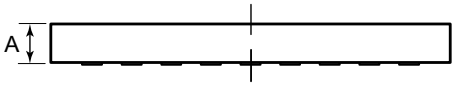
5.00x7.00mm body, 0.85mm height (max), 0.50mm pitch



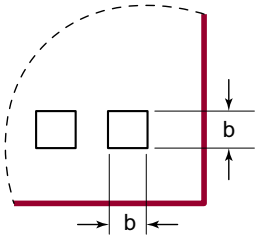
Top View



Bottom View



Side View



View A

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	b	D	E	e	e1	e2	e3
Dimension (mm)	MIN	0.75	0.20	4.925	6.925	0.50 BSC	2.00 BSC	3.50 BSC	4.00 BSC
	NOM	0.80	0.25	5.000	7.000				
	MAX	0.85	0.30	5.075	7.075				

Drawings not to scale.
Supertex Doc. #: *DSPD-22LFGALA, Version A052511.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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